UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,903	04/14/2004	Nikhil Vishwanath Kelkar	NSC1P300/P05882	7593

22434 7590 04/19/2006

BEYER WEAVER & THOMAS LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
SHANKLE, ALEXANDER	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,903	KELKAR, NIKHIL VISHWANATH	
	Examiner	Art Unit	
	Alexander J. Shankle	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-9 in the reply filed on 2-6-06 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Regarding claim 1, the phrase "as necessary" renders claims 1-9 indefinite because it is unclear whether or not the "limitation of a trimming operation that includes probing..." is a required element of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al '158 in view of Alvarez '502.

a. Regarding claim 1, insofar as definite, Kelkar '158 discloses a method comprising: providing a semiconductor wafer having a plurality of integrated circuit dice formed therein, the integrated circuit dice including a plurality of electrically conductive contact pads and electrically conductive trim pads exposed on an active surface of the wafer; forming contact bumps on a plurality of the contact pads; probing the wafer after the contact bumps have been formed, wherein the wafer probing includes, a trimming operation that includes probing the plurality of electrically conductive trim pads and trimming circuits associated with the trims pads, and a testing operation that involves probing at least some of the plurality of contact bumps to test selected functionalities of the integrated circuits (Col.4 Line 40 – Col.5 Line 40). Kelkar '158 does not disclose applying an electrically insulative undercoating to the active surface of the wafer that directly covers the trim pads while leaving at least portions of the contact bumps exposed.

i. Alvarez discloses applying an electrically insulative undercoating to the active surface of a wafer while leaving at least portions of contact bumps exposed (Fig.9 and 10A-10D).

ii. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the Alvarez method to coat the Kelkar '158 trim pads on the active surface of a wafer, leaving contact bumps at least partially exposed. The motivation for doing so would have been to

streamline semiconductor wafer production by combining trimming and functional probing steps as taught by Kelkar '158 (Col.5 Lines 8-24).

b. Regarding claims 2 and 3, Kelkar '158 and Alvarez disclose the method of claim 1 and Kelkar '158 further discloses probing for the trimming and testing operations is performed sequentially or substantially simultaneously. Kelkar '158 does not use the terminology of sequentially or simultaneously but they are implied as optional by "A wafer probe is performed to test the contact bumps for functionality and to trim the trim pads so that the die characteristics will meet the required specifications" (Col.5 Lines 8-10).

c. Regarding claims 4-9, Kelkar '158 and Alvarez disclose the method of claim 1 and Alvarez further discloses wherein the undercoating is formed from a material selected from the group consisting of: epoxies, polyimides, and silicone polyimide copolymers (¶ 76); wherein the undercoating has a final thickness in the range of approximately 0.2 and 4 mils (i.e. 5-100 microns) (¶ 68-72); wherein the undercoating is formed from an underfill material (e.g. epoxy) that is suitable for filling a region between a die and a substrate that the die is mounted to after the wafer has been diced and the die mounted to the substrate (¶ 76); wherein the undercoating is formed from a B-stageable material (e.g. epoxy) (¶ 76); wherein the undercoating is formed from a curable material, the method further comprising curing the undercoating to permanently affix the undercoating to the surface of the wafer (¶ 85); wherein the undercoating is applied by one of a spin-

on coating process, a molding process, a screen printing process and a stencil printing process (¶ 76-84).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. Pirkle et al '064, Akamatsu '290 and Eldridge '308 disclose methods that combine trimming and functional probing steps to streamline semiconductor manufacturing.

b. Lee et al '360 and Bryant et al '894 disclose methods for applying an insulative layer on an active surface leaving contact structures exposed.

USPTO CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alex Shankle whose telephone number is 571-272-3476. The examiner can normally be reached on M-F 8am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached at 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. See http://pair-direct.uspto.gov for more information about the PAIR system. Contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) for clarification on access to the Private PAIR system.

Alexander Shankle
Patent Examiner, Art Unit 2891
Semiconductors and Nanotechnology
Alexander.Shankle@uspto.gov
571-272-3476

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800